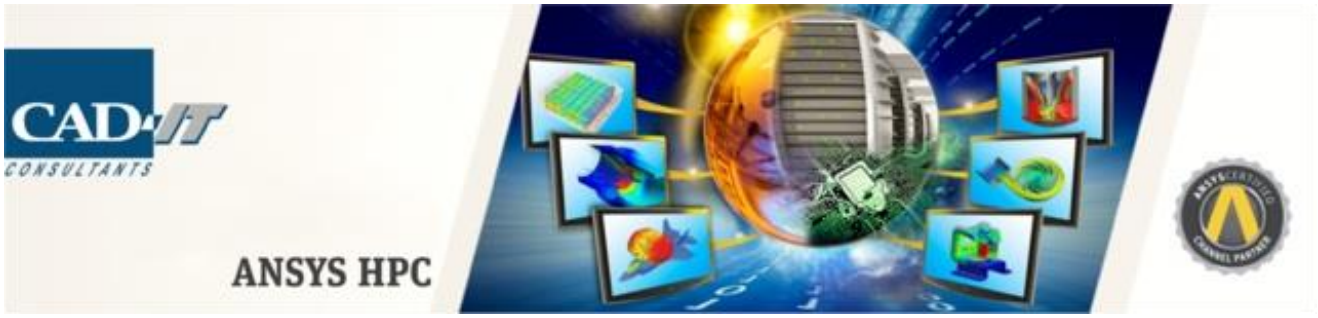

Workshop on ANSYS Productivity Tool Test Drive - HPC & DesignXplorer

16th September, 2016 | 2.00pm to 5.00pm

CAD-IT Consultants (Asia) Pte Ltd,
159 Sin Ming Road #03-05 Amtech Building,
Singapore 575625
(View map)

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An Introduction to the use of parallel processing for greater speed and productivity.

- Do you feel constrained in your simulation usage due to excessively long computational solving times?
- Do you want to leverage computational capacity to achieve faster turnaround times in a better way?
- Do you want to get higher fidelity insight from a larger or more complex simulation model?
- Are you wondering what hardware to buy?

If the answer is **YES**, then you should definitely attend this Test Drive!

You will receive best practice guidance that will help you achieve optimal performance out of your structural mechanics and fluid dynamics simulations. Guidelines will be given on CPUs, GPUs, parallel processing, interconnects, disk storage, as well as remote solving and licensing.

Benefits of using ANSYS High Performance Computing (HPC) Solutions:

- Enables the creation of large, high-fidelity models that yield accurate and detailed insight into the performance of a proposed design.
- High-fidelity simulations allow engineering teams to innovate with a high degree of confidence that their products will meet customer expectations - because their realistic simulations are predicting the actual performance of the product under realworld conditions
- Enables greater simulation throughput - using HPC resources, engineering teams can analyze not just a single design idea, but many design variations. By simulating multiple design ideas

concurrently, R&D teams can identify dramatic engineering improvements early in the design process, prior to and more effectively than physical prototyping alone

Presenter Profile:

Dr. Lee Yong Jiun is a Technical Applications Engineer at CAD-IT. He graduated from National University of Singapore with a PhD in Mechanical Engineering. His Research Focus was on Thermal management in Electronics, primarily using ANSYS solutions. Yong Jiun was with the Institute of Microelectronics and served as Project Leader to design, fabricate and characterize a package level thermal management solution. He has also worked for INTEL

Technology as Assembly Technology Development Engineer, where his primary responsibility of the job was to develop a robust flip chip assembly process for Intel next generation chipsets. Yong Jiun is responsible for the technical support of ANSYS CFD solutions.

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